

**REMARKS**

Claims 1, 3, 5, 7, 9, 11, 17, and 19 are presented for examination. Claim 1 has been amended to incorporate the subject matter of claims 2 and 14 cancelled without prejudice or disclaimer. Claims 13 and 15 have been cancelled as being redundant because they recite the subject matter incorporated in independent claim 1. Claims 4, 6, 8, 10, 12, 16, 18, 20-24 have been cancelled as being dependent from the cancelled claims.

Claim 1, as amended, recites a cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory. The cache memory system comprises:

- a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and

- a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware.

The claim specifies that:

- the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control,

- when a cache miss happens at the time of the software control, the processor automatically causes the hardware cache controller to perform the hardware control, and

- the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

Claims 1-6, 9-10, and 17-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Fujiwara publication entitled “A Custom Processor for the Multiprocessor System ASCA.” Dependent claims 7-8 and 11-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Handy publication entitled “The Cache Memory Book.” Dependent claims 13-16 and 21-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Hallnor publication entitled “A Fully Associative Software-Managed Cache Design.”

It is respectfully submitted that the prior art of record neither teaches nor suggests the features recited in claim 1.

In particular, for software control, locations for storing cache lines in a cache memory and management of the cache lines are different than for hardware control. Usually, when the software control is automatically switched to the hardware control, some of the cache lines in the cache memory, that have content different from the content of the main memory, are completely written back into the main memory and then, all the cache lines are invalidated. This causes an extremely large overhead for the processing, resulting in deterioration of efficiency.

By contrast, claim 1, as amended, recites that whereas the management of the cache lines by the software control is performed by a set-associated method for multiple ways, the cache lines management by the hardware control is performed by using a fully associative method for at least one way in the multiple ways.

For example, the software control may perform management of the cache lines by the set-associated method for the first to third ways of the four ways in the same manner as the hardware control, which may perform the cache lines management by the fully associated method only for the fourth way of the four ways. Therefore, when the software control is automatically switched

Serial No.: 10/076,625

to the hardware control, the write back and invalidation may be performed only for the fourth way. As a result, the overhead in this example is reduced to one fourth of the conventional method described above.

Hence, the present invention makes it possible to reduce deterioration of efficiency caused by automatic switching from the software control to the hardware control.

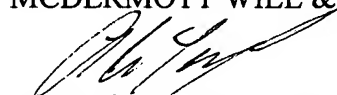
As the cited references neither teach nor suggest the subject matter of claim 1, it is submitted that the claims, as amended, overcome the rejections of record.

In view of the foregoing, and in summary, claims 1, 3, 5, 7, 9, 11, 17, and 19 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



Alexander V. Yampolsky  
Registration No. 36,324

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
202.756.8000 SAB:AVY:men  
Facsimile: 202.756.8087  
**Date: September 22, 2004**